REMARKS

Summary of Amendments and Status of Claims

Claims 1 and 2 have been amended to more particularly point out and distinctly claim the subject matter of the present invention, and also to address the Office's objection to these claims.

Claims 11 and 12 have been amended slightly for editorial clarity, as a basis for two new dependent claims depending respectively from each.

New dependent claims 13 and 14 have been added to recite an additional feature of the instant invention, which is set forth exemplarily in paragraphs [0023] and [0024] of the present specification.

Claims 3 and 5 are withdrawn, and claims 4 and 6-10 are canceled.

- **Claims 1, 2 and 11-14 are pending.**

Claim Objections

Claims 1 and 2 were objected to for lack of clarity in the recitation "one or more selected from Si, Cr, Mn . . . ." This recitation has been amended to generically classify the group as "elements," which term is among the identifiers suggested by the Examiner, and is as given in the present specification, in paragraph [0131], which states, "If the residual quantity of metal elements, including metalloid Si, is 100×10^{10} atoms (at)/cm^2 or less, the wafer is sufficiently clean to be useable as a device substrate."

It is believed that the appropriate correction has thus been made.

Claim Rejections – 35 U.S.C. § 103

Claims 1, 2, 11 and 12: Wilk et al. '660 in view of Freeouf et al. '829, and further in view of Yang et al. '810

Claims 1, 2, 11 and 12 were rejected as being unpatentable over U.S. Pat. App. Pub. No. 2004/0067660 in the name of Wilk et al., in view of U.S. Pat. No. 5,508,829 to Freeouf et al., and further in view of U.S. Pat. App. Pub. No. 2004/0149810 in the name of Yang et al.

Wilk et al. is alleged to disclose "a gallium-nitride substrate onto which film has been epitaxially grown," and to disclose the film-bearing substrate as being "contaminated

on its epitaxial-film side at a density level of from 15×10^{10} to 10×10^{11} atoms/cm^2." As will be demonstrated below, what constitutes "film" and "contamination" according to *Wilk et al*. stands in contradistinction to what these terms clearly signify according to the present invention as claimed.

Wilk et al. is directed to forming, by atomic layer deposition, an insulating layer, which may function as a passivation layer, onto III-V semiconductor substrates "to produce an active device where the substrate has an unpinned Fermi Level" (paragraph [0015]). The active devices are metal oxide semiconductor field effect transistors (MOSFETs), although the formation of a set of capacitors from the same ALD-deposited insulating layer on a III-V substrate is also described. The possibility of forming metal semiconductor field effect transistors (MESFETs) onto an insulating-layer-bearing III-V substrate formed according to the *Wilk et al*. method is also mentioned (paragraph [0038]).

Although the thrust of *Wilk et al*. is thus the ALD deposition of MOSFET insulating layers on GaAs substrates, paragraph [0017], the first of the two cited by the Office, does mention, "In certain . . . embodiments . . . the substrate comprises GaAs, InP, or GaN." Nevertheless, despite the mention of GaN as a substrate for the ALD deposition of MOSFET insulating layers, *Wilk et al*. in no wise is concerned with the manufacture of light-emitting devices, as in contrast is the present invention. Nowhere does *Wilk et al*. disclose, teach, or even suggest forming a light-emitting-device-forming film onto a gallium nitride substrate.

The Office then turns to *Yang et al*. to show a teaching of "how traditional light-emitting diodes use III-V compounds by using epitaxial wafer growth technology," and that utilizing "III-V compounds for light-emitting diodes" is "conventional and well-known." Indeed, the Office could have turned to any of innumerable sources other than *Yang et al*. to show the desirability of forming III-V based light-emitting devices. Yet even if a person skilled in the art were to attempt to build a light-emitting device on a *Wilk et al*. substrate, that person would not arrive at the present invention, for at least the following two reasons.

I. *Wilk et al*. is utterly silent as to substrate surface preparation. In particular, *Wilk et al*. mentions nothing about polishing the III-V substrates prior to ALD formation of insulating layers onto the substrates. Nor does *Wilk et al*. mention anything whatsoever as to the smoothness or flatness of the substrates. In fact, paragraph [0017] of *Wilk et al*. states, "Any conventional III-V semiconductor substrate may be used in the present invention." One must conclude, then, that as of the October 3, 2002 filing date of *Wilk et al*., the state of the art of device-formation onto III-V substrates was, as noted in paragraph [0006] of the present specification—whose priority dates to October 27, 2003, more than a year after *Wilk et al*.—"[O]ne in which films are grown onto the crystal as it is, without polishing or etching."

   Moreover, paragraph [0017] of *Wilk et al*. continues,

> In other advantageous embodiments, the III-V semiconductor substrate has an epiready surface thereon. The term epiready surface as used herein refers to a III-V semiconductor substrate having a surface, comprising the same III-V material, that has been grown by conventional molecular beam epitaxy, for example. Those of ordinary skill in the art are aware of the procedures for preparing epiready III-V semiconductor substrates.

Yet while *Wilk et al.* seems confident that persons skilled in the art will know how to prepare epiready substrates, a search of the Office's patent and published patent application databases turns up only five and six documents, respectively, on the keyword "epiready." Accordingly, it must be wondered whether a *prima facie* case can be made that a substrate said to be "epiready" would be understood by a person skilled in the art to mean that the substrate has been polished, and polished to the minimum level of smoothness required in order to form a light-emitting device onto the substrate.

As the present specification makes abundantly clear, GaN conventionally had not been polished in preparation for device formation, because although conventional polishing techniques can be employed on GaN substrates, the process-transformed layer left by the polishing operation could not be removed by conventional techniques, because, as noted in paragraph [0010] of the specification, "As yet . . . there is no GaN etching technology. For the most part, GaN cannot be etched with chemically active substances."

Wilk et al., paragraph [0019], does mention, "The method . . . may further include a step . . . of performing a thermal anneal of the III-V semiconductor substrate before depositing the insulating layer," yet as pointed out earlier, *Wilk et al.* never mentions polishing at all. One of the patents that turns up on the keyword search just described, U.S. Pat. No. 7,060,620, does give a minimum level of smoothness for a substrate said to be epiready—2 nm *rms*—and interestingly enough, that smoothness level is said to be attained by annealing. Hence, it may be fairly concluded that according to *Wilk et al.*, annealing a III-V semiconductor substrate is sufficient to make the substrate epiready.

It must be concluded that *Wilk et al.* is not concerned with polishing III-V substrates to a mirrorlike, planar finish because *Wilk et al.* is only concerned with transistor formation, not light-emitting device formation. That is, a person skilled in the art would readily understand that semiconductor substrates for forming transistors do not require the degree of planarity that semiconductor substrates for forming light-emitting devices require. One reason why is because transistors do not require nanometer-order quantum well layers to be deposited on the semiconductor substrates, whereas light-emitting devices typically require such layers to be deposited on the substrate.

In sum, the fact that *Wilk et al.* is silent as to substrate surface preparation apart from annealing, and the fact that *Wilk et al.* is concerned exclusively with

transistor fabrication mean that *Wilk et al.* is not even enabling for the formation of light-emitting devices on III-V substrates.

As explained in numerous instances in the present specification, the present invention involves a gallium nitride substrate that has been polished to a mirrorlike, planar finish. Indeed, the thrust of the present invention is coping with the process-transformed layer left by the polishing operation. In sharp contrast to *Wilk et al.*, then, the present invention as set forth in claims 1 and 2 of the present application is "[a] gallium-nitride semiconductor substrate having a mirrorlike, planar surface onto which a light-emitting-device-forming film has been epitaxially grown."

II. Second, the "contamination" that the Office alleges that *Wilk et al.* describes is stated in paragraph [0027], the second of the two cited by the Office, to be not contamination but "trap density." Paragraph [0027] of *Wilk et al.* goes on to define "trap density" as referring "to electrically active defects in the III-V semiconductor substrate that are capable of trapping charge carriers, resulting in Fermi level pinning, low transconductance and other deleterious effects well known to those of ordinary skill in the art." Thus, in effect, the Office is alleging that the electrically active crystalline defects that *Wilk et al.* seeks to reduce are tantamount to the metal and metalloid surface contaminants that the present invention seeks to reduce.

The trap density described in *Wilk et al.* cannot be equated with the range of minimized substrate-surface contaminant density according to the present invention as claimed. The reasons why are at least twofold.

One, trap density is a bulk, not surface property, of a substrate, as is clear from the discussion in *Wilk et al.* of Fermi level pinning. While paragraph [0015] of *Wilk et al.* does state, "[I]t is thought the deposition of the insulating layer via ALD helps to substantially reduce traps at the surface of the substrate that lead to pinning," it is clear from the following earlier statement, in paragraph [0003], that "at the surface" means near, not on, the surface: "It is thought that the Fermi level of the GaAs semiconductor substrate at an interface between the GaAs and the insulating layer is substantially pinned, arising from a poor-quality interface characteristic of III-V surfaces."

Two, "pinning" is defined as "the hindering of motion of dislocations in a solid . . . by impurities which collect near the dislocations, resulting in a large energy barrier being imposed against the motion of the dislocations" (McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition.) It follows, then, that the electrically active defects referred to in *Wilk et al.* become traps because impurities collect near them, and while thus as traps the defects capture (possibly metal/metalloid) charge carriers, the traps are not themselves metal/metalloid impurities.

Claims 1 and 2 recite, "the gallium-nitride substrate therein contaminated on its epitaxial-film side by one or more elements selected from Si, Cr, Mn, Fe, Ni, Cu, Zn and Al at a density level of from 15×10^{10} to 10 {or 5, in claim 2} $\times 10^{11}$ atoms/cm^2." (Emphasis added.)

In an apparent attempt to make up for the *Wilk et al.* deficiency just pointed out, the Office cites *Freeouf et al.*, which describes "Cr inclusions" functioning to trap charge carriers. Thus, the Office's rationale for combining *Wilk et al.* with *Freeouf et al.* seems to be that if *Wilk et al.* describes only defects (dislocations) acting to trap charge carriers, because *Freeouf et al.* teaches that Cr inclusions can function to trap charge carriers, the Cr inclusions of *Freeouf et al.* can substitute for such defects as taught by *Wilk et al.* And since the Office cites *Wilk et al.* allegedly to demonstrate disclosure of a predetermined level of III-V substrate contamination, the Office seems to be reasoning that that a person skilled in the art would understand that the contamination that *Wilk et al.* describes could, according to *Freeouf et al.*, be Cr contamination.

Yet as noted above, it must be that the dislocations of *Wilk et al.* act as charge-carrier traps because they have been pinned by metal impurities. If, as the Office seems to suggest is the rationale for combining *Wilk et al.* with *Freeouf et al.*, the contaminants of *Freeouf et al.* could be the pinned dislocations of *Wilk et al.*, then by that rationale, the Office would be alleging the existence of a III-V substrate in which metal impurities would be pinning metal impurities.

Moreover, even if the Cr inclusions of *Freeouf et al.* could be said to be tantamount to *Wilk et al.*'s pinned-defects-as-traps, for the reasons given above in discussing the relevance of traps as described in *Wilk et al.* such inclusions nonetheless would not in any way be tantamount to the metal contaminants that the present invention is concerned with.

In short, to suggest, as the Office seems to be in citing *Freeouf et al.*, that a person skilled in the art would read, in light of *Freeouf et al.*, *Wilk et al.*'s trap density as tantamount to a density of metallic inclusions—and therefore contaminants as claimed in the instant application—is technically off-base.

Wilk et al. in combination with *Freeouf et al.* cannot possibly arrive at the invention set forth in claims 1 and 2 of the instant application:

> A gallium-nitride semiconductor substrate having a mirrorlike, planar surface onto which a light-emitting-device-forming film has been epitaxially grown, the gallium-nitride substrate therein contaminated on its epitaxial-film side by one or more elements selected from Si, Cr, Mn, Fe, Ni, Cu, Zn and Al at a density level of from 15×10^{10} to 10 {5} $\times 10^{11}$ atoms/cm^2.

Conclusion

The cited references, *Wilk et al*. in combination with *Yang et al*. and *Freeouf et al*., do not meet the limitations of the present claims—no matter how stretched an interpretation of any or all of these references a person skilled in the art might even be inclined to make. Claims 1 and 2 being patentably distinct from the cited combination of references, it follows that their respective dependent claims 11 and 12 are patentably distinct as well.

Accordingly, Applicant courteously urges that this application is in condition for allowance. Reconsideration and withdrawal of the rejections is requested. Favorable action by the Examiner at an early date is solicited.

Respectfully submitted,

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